mented transistor sections. In this embodiment, a single dummy pillar is centrally located between the four rounded ends of adjacent pairs of transistor segments over the two sections. In the example shown, for every N (where N is an integer greater than 1) racetrack segments or structures in a section **30** of the transistor comprising die **21**, there are a total of N−1 dummy pillars **33**.

FIG. **4**A illustrates yet another example layout of the vertical HVFET structure shown in FIG. **1**. FIG. **4**B is an expanded view of one portion of the example layout shown in FIG. **4**A. Pillars **17** and oxide region **15***b* are just shown for clarity reasons in the expanded view of FIG. **4**B. In this example, the transistor segments comprising the HVFET of semiconductor die **21** are alternately shifted by half of the length of each racetrack segment, resulting in racetrack transistor segments that are alternately associated with upper transistor section **40***a* and lower transistor section **40***b*. In other words, each of the transistor segments of a row of section **40***a* is separated by a pair of the transistor segments of section **40***b*, the pair being arranged in an end-to-end relationship in the x-direction.

It is appreciated that the alternate shifting of the segments may be any fraction of the segment length. In other words, shifting of the segments is not limited to 50% or half the length. Various embodiments may comprise segments alternately shifted by any percentage or fraction ranging from greater than 0% to less than 100% of the length of the transistor segments.

In the example of FIGS. **4**A & **4**B, the dielectric regions **15***b* of alternating ones of the transistor segments in respective sections **40***a* & **40***b* are merged. In the specific embodiment shown, the rounded ends of the transistor segments associated with different adjacent sections overlap or are merged such that field plates **19***b* of the adjacent sections are merged at the ends (in the x-direction). Also, the extended straight side portions of field plates **19***b* of alternating transistor segments of different sections are merged along a substantial length of each segment. It is appreciated that regions **15***b* and **19***b* may be merged with or without a dummy pillar (or isolated dummy silicon pillars) between the respective sections.

Although the above embodiments have been described in conjunction with a specific device types, those of ordinary skill in the arts will appreciate that numerous modifications and alterations are well within the scope of the present invention. For instance, although HVFETs have been described, the methods, layouts and structures shown are equally applicable to other structures and device types, including Schottky, diode, IGBT and bipolar structures. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

We claim:

1. An apparatus comprising:

a plurality of transistor segments arranged on a die, each transistor segment having a racetrack shape with a length elongated in a first lateral direction and a width in a second lateral direction, each transistor segment including:

a pillar of a semiconductor material, the pillar including an extended drain region that extends in a vertical direction through the die;

a first and second dielectric regions disposed on opposite sides of the pillar, respectively, the first dielectric region being laterally surrounded by the pillar, and the second dielectric region laterally surrounding the pillar;

first and second field plates respectively disposed in the first and second dielectric regions;

wherein the transistor segments are arranged into a plurality of sections, a first section comprising a first row of transistor segments arranged in a side-by-side relationship in the second lateral direction, and a second section comprising a second row of transistor segments arranged in the side-by-side relationship in the second lateral direction, the second dielectric region of each transistor segment of the first section being merged with the second dielectric region of each transistor segment of the second section.

2. The apparatus of claim **1** wherein the transistor segments of the first and second sections are each separated in the first lateral direction by at least one dummy pillar of the semiconductor material.

3. The apparatus of claim **2** wherein the at least one dummy pillar comprises a single dummy pillar that separates the first and second sections.

4. The apparatus of claim **3** wherein the single dummy pillar adjoins, in the first lateral direction, a rounded end of the second dielectric region of each transistor segment of the first and second sections.

5. The apparatus of claim **1** wherein the second dielectric region is terminated at each end in the first lateral direction in a rounded end.

6. The apparatus of claim **1** wherein the first and second field plates are fully insulated from the extended drain region, the first field plate being laterally surrounded by the pillar, and the second field plate laterally surrounding the pillar.

7. An apparatus comprising:

a plurality of transistor segments arranged on a die, each transistor segment having a racetrack shape with a length elongated in a first lateral direction and a width in a second lateral direction, each transistor segment including:

a pillar of a semiconductor material, the pillar including an extended drain region that extends in a vertical direction through the die;

a first and second dielectric regions disposed on opposite sides of the pillar, respectively, the first dielectric region being laterally surrounded by the pillar, and the second dielectric region laterally surrounding the pillar;

first and second field plates respectively disposed in the first and second dielectric regions;

wherein the transistor segments are arranged into a plurality of sections, a first section comprising a first row of transistor segments arranged in a side-by-side relationship in the second lateral direction, and a second section comprising a second row of transistor segments arranged in the side-by-side relationship in the second lateral direction, the transistor segments of the first and second sections each being separated in the first lateral direction by a plurality of dummy pillars of the semiconductor material, each dummy pillar being centrally located between rounded ends of first and second adjacent pairs of transistor segments of the first and second sections, respectively.

8. The apparatus of claim **7** wherein the pillar further comprises a source region disposed near a top surface of the die, and a body region that vertically separates the source region from the extended drain region.

9. The apparatus of claim **8** further comprising a gate disposed within the first and second dielectric regions adjacent the body region, the gate being insulated from the body region and the first and second field plates.